SWITCH MODULATION TECHNIQUES

REPORT No.1

SIGNAL CORPS CONTRACT No. DA 36-039-SC-87353

DEPARTMENT OF THE ARMY TASK No. 3A99-09-002-05

PREPARED FOR

**U.S. ARMY SIGNAL RESEARCH
AND DEVELOPMENT LABORATORY**

FORT MONMOUTH, NEW JERSEY

FIRST QUARTERLY PROGRESS REPORT

15 JULY 1961 to 31 OCTOBER 1961

GENERAL ELECTRIC

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LIGHT MILITARY ELECTRONICS DEPARTMENT • ADVANCED ELECTRONICS CENTER

CORNELL UNIVERSITY INDUSTRY RESEARCH PARK • ITHACA • NEW YORK

SWITCH MODULATION TECHNIQUES

THE FREQUENCY MODULATED SELF-STABILIZING INVERTER AND ITS APPLICATION TO A REGULATED AC TO DC POWER SUPPLY

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Prepared by Francisc C. Schwarz

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I. PURPOSE

Work on this contract is directed toward an investigation of potential improvements in the area of power supplies in the light of advancements of circuit concepts and technology of components.

Improvements are sought with respect to higher reliability and efficiency, associated with reductions of physical size and weight. Another intended improvement is seen in a relatively wide range of adaptability of these power supplies to supply line voltages and frequencies. The exclusive use of silicone semiconductor devices as nonlinear resistive two-terminal and three-terminal circuit components and the application of advanced concepts in the design of iron core devices contribute to the establishment of all solid-state circuits for the purpose under consideration.

Theoretical and experimental studies (Item 1) will be reinforced by construction of two different experimental models, to conform to the specifications as listed in the following:

Item 2:

Power Converter ac to dc

Input: Single phase 115/230 volts ac rms ± 10%, 50/60/400 cps ± 5%

Output: 26 volts dc, 0 to 10 amp dc

Regulation: ± 1% under any combination of line voltage variation and no load to full load current variations

Ripple: 0.5% peak to peak

Ambient Temperature: -55 to +65 C

Load: Resistive load

Item 3:

Power Converter ac to dc, as specified for Item 2, except for:

Output: 22 to 30 volts dc, 0 to 20 amp dc, continuously adjustable

This work was initiated by a preliminary study phase into the fourth month of this program, and carried out at the Advanced Electronics Center of the Light Military Electronics Department in Ithaca, New York, and the Electronics Laboratory in Syracuse, New York, both within the Defense Electronics Division of the General Electric Company.

Two different concepts were studied during this period and discussed between representatives of USASRDL, Ft. Monmouth, and the General Electric Company during a conference in Ithaca on October 27, 1961. By agreement of all parties, work will be continued in Ithaca and directed toward a construction of a breadboard model conforming to the specifications of Item 2, and applicable to modifications to conform to the specifications of Item 3. This phase will essentially cover the second quarter of the program, while the effort during the remainder of the available time will be directed toward construction of the experimental models, as called for by the contract, in addition to appropriate analytical work and technical writing.

II. ABSTRACT

Two concepts were studied with regard to this program, as intended. The FM-SS inverter developed in Ithaca, New York, shows promise for successful completion of this program and work in that direction will be continued. The Tap Switch Modulation approach as studied in Syracuse was abandoned, as recommended by the Syracuse technical personnel, showing a too high ratio of complexity to advantages gained.

Progress of work on the FM-SS inverter was demonstrated in Ithaca by operation of a breadboard near rated power (Item 2) in conjunction with a verbal presentation. This power modulator is self-stabilizing, self-protecting, operates as an active filter section with respect to the source ripple, has automatic controlled rectifier turn-off, under elimination of commutation currents, and uses no energy-destructive (damping) networks. These properties indicate a lightweight, reliable power supply with relatively high efficiency. Attenuation of the source ripple by a factor four was attained experimentally by active filtering of the FM-SS inverter, and there are efforts underway for further improvement. A reduction of size and weight of at least two-thirds, compared to a conventional power supply with equal performance and efficiency, is expected as a result of this program.

Problems arising from fast rising wave forms and high repetition rate in the output rectifier were overcome by proper choice of fast switching diodes and adequate circuitry. Other problems entailed by relatively light loading, in the order of 10 percent, are being worked on presently.

III. CONFERENCES

Two conferences with representatives of USASRDL, Fort Monmouth, N.J., and the General Electric Company participating, as stated under Purpose were held in July, 1961 at Fort Monmouth and on October 27, 1961 in Ithaca, N.Y., respectively.

The first conference had the object of reaching a mutual understanding on procedural matters, and the course of technical efforts. A program was adopted to pursue the study of two different and independent technical approaches to the task as stated by the underlying contract, at the Electronics Laboratories in Syracuse, and the Advanced Electronics Center in Ithaca, respectively. This was to continue into the fourth month of the contractual program (10/15 to 11/15, 1961), when a second conference was to be held for the purpose of continued contact and exchange of information on any administrative questions and technical matters. It was, furthermore, intended to reach by that time an understanding as to which of the technical approaches should be continued from then on toward the goals of this program.

The second meeting took place in Ithaca, on the date stated before. The representatives of USASRDL were informed of the progress of the technical work carried out at both locations of the General Electric Company by verbal presentations, given by the technical personnel carrying out the work. Furthermore a functional breadboard model of an amplifier, output rectifier, and filter built in Ithaca according to the principles described under Factual Data (IV. A, B, C, E) of this report and operating near the rated power level of Item 2 of the contract was demonstrated. It was acknowledged by the representative of USASRDL, that the program is progressing as planned, both in technical work and in its financial aspects. It was, furthermore, jointly agreed to continue further work in Ithaca and terminate the program in Syracuse. Motivation for that decision was based on a considerable ratio of circuit complexity to weight improvements of the tap switch modulation technique.

IV. FACTUAL DATA

A. General System Considerations

A regulated power supply will convert unregulated power as supplied by the source and of a certain character into regulated power of the same or a different desired character. This device then controls the flow of energy from source to load per unit of time in a predetermined way, including amount and time variation of the power flow.

An application of these formulations to the regulated ac to dc power supply describes the task of this device to convert ac into regulated dc with certain predetermined variations, like regulation, ripple, transient response, etc. Three of these functions appear to contribute decisively to the reliability, quality, and physical size of the system: ac to dc conversion, regulation including voltage level change, and wave shaping (filtering). The system components that bring about these functions are referred to as rectifier, amplifier, and filter. These well-known facts are restated here for convenience for a reconsideration of the general problem.

Static devices have, in general, adhered to distinction of the three functions enumerated above and attacked the respective problems individually. In that case, size and weight of the power supply were essentially determined by the frequency of the supply source, and the desired performance characteristic. The latter will include the type of amplifier used, efficiency, etc.

It appears that size and weight of an amplifier can be reduced by the use of a self-oscillating circuit instead of the driven amplifier operating at the source frequency. An implementation of this principle by use of an amplifier and an inverter in cascade is quite common and shows at times improvements over the driven amplifiers. The pursued goal is to have an increase in operating frequency resulting in a reduction of weight and size of iron core devices, e.g., transformers.

The duality of the cascaded arrangement leads logically to the concept of the Power Modulator which combines the amplifying and inverting function into one device by pulse width modulated inversion (1).

These amplifiers operate in the kilocycle range, and permit a substantial reduction in size and weight of one of the main contributors on that account, the transformer. This level changing device now operates in the kilocycle range instead of one of the conventional frequencies (50/60/400 cps). Previous work (2) has shown that an increase in operating frequency of power transformers leads to substantial size and weight reductions of these devices, associated with an improvement of performance (efficiency and regulation). The latter results from the fact that increases in specific losses are more than offset by reduction in volume, with proper choice of materials, and design principles.

The advantage of weight reduction of the amplifier does, however, not affect considerations of the required filter size, unless the amplifier contributes to the filtering process. One such amplifier that reduces the filter size by improvement of wave shape by transformation of the incoming sine wave to a quasi-square wave is the shunt-loaded magnetic amplifier (3), which, however, operates at the source frequency and does not offer the advantages of higher frequency operation. Recent work on the Amplitude-Modulated Magnetic Amplifier to overcome that limitation is currently in progress. Another amplifier striving toward an improvement of the power ripple employs a transformer tap switching technique which increases the transformation ratio during the lower portions of the voltage ripple, tending to improve the amplifier output wave in that way.

A different approach to the problem of filtering is gained by incorporation of the amplifier into the filter as an active filter section that diminishes the ripple of the power flow and furthermore counteracts it by ripple opposing modulation. This is to a certain extent implemented in a series regulator and constitutes a long standing practice in power supply design. The approach to be discussed is distinguished from the series regulator as being an essentially nonresistive network, rather than a variable series resistance, and a self-oscillating power modulator.

The desired nondissipative character of that power modulator implies that no variable resistance elements are used as such, and all encountered resistances are inherent in the shortcomings of physical components, rather than planned circuit features. This restricts the function of semiconductors in the circuit to a strict on-off operation, indicating pulse duration modulation for control. One feature was added to the pulse duration modulation by endowing this power modulator with a self-stabilizing function to operate as a Pulse Duration Modulated Self-Stabilizing (PDM-SS) amplifier (2). An amplifier that shows certain similarity to the PDM-SS amplifier is being used for the present program. The philosophy of operation and the physical implementation have been substantially modified.

This Frequency-Modulated Self Stabilizing (FM-SS) Inverter, or Power Modulator (4) is being used as an active filter section within a three-section filter composed by:

(a) an input filter section performing coarse filtering of the 100 cps rectified incoming ac voltage wave;

(b) an active filter section formed by the FM-SS inverter and counteracting the ripple of power flow by opposing modulation to that power flow;

(c) an output filter stage that filters the alternating current generated by the power modulator at kilocycle speed, and acts as the third filter section with respect to the original 100 cps ripple frequency.

This arrangement, including rectifiers, is illustrated in Figure 1.

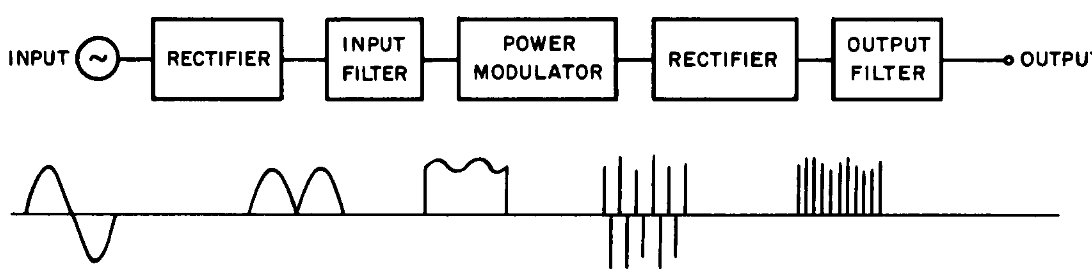

Figure 1. Successive voltage wave shaping

The purpose of the first (input) filter section is to provide a definite range of excursions of the dc voltage feeding the power modulator, at a minimum expense of size and weight. For the present application a ripple attenuation between 8 and 10 was considered such that the dc voltage as fed into the power modulator would vary less than ± 10 percent (peak). The power modulator, acting as a filter section performs two functions: it (a) contributes to the overall attenuation by a factor of at least four when referred to its output voltage, while the amplitude ripple attenuation is about four times that factor, and it (b) prevents interdependence of the first and third filter section, rendering the product of individual attenuations a true measure of total attenuation of the filter network. The present contract calls for a maximum output ripple of 0.5 percent peak to peak or 0.25 percent amplitude, which indicates an overall attenuation of about $67/0.25 \cong 268$, thus leaving a burden of an attenuation of about 7 on the output filter. It will be shown that an attenuation of about 3 referred to 100 cps coincides with a smooth operation of the hf modulator wave, so that the remaining factor of 2.3 will be attained by an improvement of active filtering of the modulator -- as experimentally proven feasible -- or an increase of the output filter size.

A reduction of the filter size by better than a factor of four is attained in one case, taking into consideration the validity of the attenuation product of the successive stages. In the other case this reduction will be improved to a factor of better

than eight. Improved design and techniques with respect to iron core devices should bring about a further substantial improvement in reduction of size and weight of these devices.

To summarize, it is the duality of functions of the power modulator that reduces the transformer size by static modulation acting as an inverter, and reduces the overall filter size by dynamic modulation, operating as an active filter section and regulator.

The system is now determined by the arrangement as shown in Figure 1 in accordance with the conclusions reached. The block diagram of the actual system will show some additions of implementary necessity, but preserve the expressed concept.

B. The Frequency Modulated Self-Stabilizing (FM-SS) Inverter

This is an inverter type amplifier with a characteristic triangular output voltage waveshape controlled by the repetition rate of the individual periods. Amplitude and duration of these individual periods of output voltage depend upon design of the power circuit, input voltage, and loading and occur free of interference by the amplifier control. The amplifier will then delay the complete next period until a time that will correspond to a predetermined average output voltage. This amplifier is compared below with a conventional magnetic amplifier, to clarify the concepts involved, although the actual waveshape involved may be of a different character. Figures 2(a) and (b) show the rectified load voltage wave originated

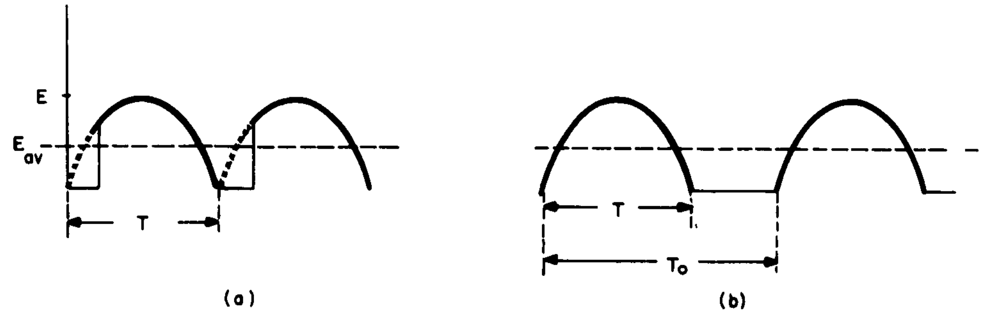

Figure 2. Average output voltage control by the principles of (a) the conventional magnetic amplifier, (b) the FM-SS amplifier

by (a) a conventional magnetic amplifier and (b) the FM-SS inverter respectively. The objective is the same in both cases: to derive from a sine wave with amplitude E and a (half) period T an average voltage E_{av}. In case (a) a repetition rate $1/T$ of the sine half wave is maintained and an appropriate portion of that half wave eliminated by firing delay to the satisfaction of the desired average voltage E_{av}. In case (b), the entire sine half wave is applied unaltered to the load, and then the appearance of the next half wave is delayed until a time $T_o > T$ to the satisfaction of the same desired average voltage E_{av}, as before. The voltage wave in case (b) cannot originate from an alternator with a given rotational speed, but stems from a relaxation power oscillator that will be discussed here.

A brief statement of the objects of operation will precede a functional description of the circuit. One purpose of the characteristic operation of the FM-SS inverter is the complete suppression of commutation currents inherent to inverter operation, and the purposeful (nondissipative) use of energies present in intended or tolerated storage elements at the termination of on-periods of operation. These two properties constitute a unique feature of this circuit, and entail an automatic, nonenforced, turn-off technique of controlled rectifiers. The latter property is found in the RC-Inverter (5), whose development preceded the FM-SS inverter, but involved commutation currents, though on a moderate level.

The power circuit of the FM-SS inverter used for a dc power supply is shown in Figure 3 and is identical with that of the RC-inverter mentioned above, except for the transformer T which may or may not be saturable for certain applications.

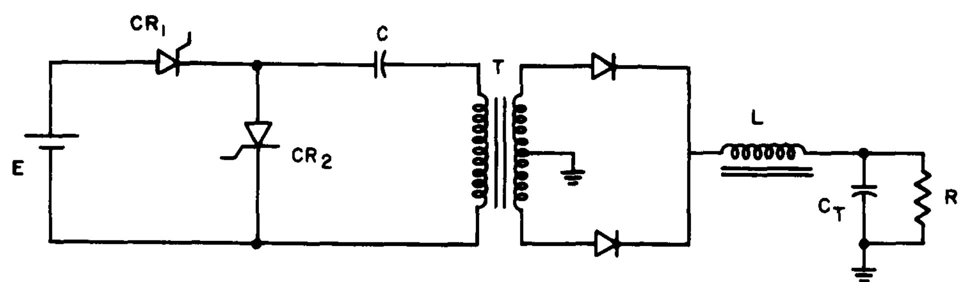

Figure 3. Power circuit of the FM-SS modulator operating in a dc to dc power supply

Consider steady-state operation with a constant load current flowing in output inductor L. When transformer T is connected to the source E via controlled rectifier CR_1 and capacitor C, then the constant current flowing in L and in the respective secondary winding of transformer T will be matched by a constant source current of proper magnitude, corresponding to the winding ratio of the transformer. This constant current is also the capacitor C current and is related to the capacitor voltage e_C essentially by

$$i_L' = C \frac{de_c}{dt} \tag{1}$$

where

i_L' is the constant load current, i_L, as reflected into the primary current of transformer T.

Since i_L was understood to be essentially constant (due to the relatively large inductor L), i_L' can be considered constant in turn and the capacitor voltage

$$e_c(t) = e_c(0) + \frac{t}{c}\, i_L' \qquad 0 < t < T \tag{2}$$

where

$e_c(0)$ is the capacitor voltage at time zero, when the cycle starts and CR_1 fires

T is the duration of the on-period

This means that the capaciter voltage time wave $e_c(t)$ is a ramp for each on-period when driven from the source E.

Conversely when CR_1 is -- somehow -- turned off at time T, and CR_2 turned on at time $T_o > T$, then it is seen by analogous consideration that

$$e_c(t) = e_c(T) - \frac{i_L'}{C}\, t \qquad T_o < t < T_o + T \tag{2a}$$

by polarity relations of primary to secondary windings. The capacitor voltage time wave $e_c(t)$ is again a ramp with slope of equal magnitude and reverse sign when operating with respect to ground. During times $T < t < T_o$ no change of capacitor C voltage takes place, both CR's being open, and the voltage time wave on capacitor C is illustrated in Figure 4.

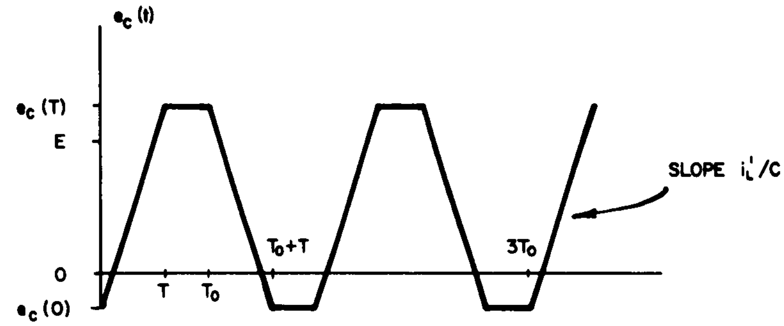

Figure 4. Voltage time wave e_c (t) on capacitor C

The wave shape in Figure 4 shows an overshoot of e_c over the source voltage E at time T, which has not been discussed so far. When e_c reaches the potential E, the drive from the supply source subsides, and inductor L assumes the role of a driving current source by virtue of its stored energy. Current i_L will continue to flow as being reflected through transformer T into the primary windings and capacitor C will continue to charge. However, the transmittal of this direct current occurs now by ac coupling (through transformer T) and has accordingly to subside after a transient phase, but by then the capaciter voltage e_c exceeds the source voltage E, and CR_1 turns itself off with an endeavor of the circuit to reverse the current i_L'.

The undershoot of e_c under the reference level toward the end of the reverse cycle is readily seen by analogous reasoning, and the automatic turn-off of CR_2 thus explained. It should be noted that all energy storage elements, including the leakage reactance of the transformer continue through the turn-off phase to perform their assigned task or shift the stored energy into another storage element such that essentially no need for damping or destruction of energy exist under normal operating conditions. All energy existing in the secondary circuit continues to flow into the load, and all energy stored in elements of the primary circuit will be eventually stored in capacitor C for further purposeful use during the succeeding period.

It has been shown that this operation does not involve any commutation (turn-off) currents and essentially all stored energy is returned to purposeful use. The aim of these initially stated objects is an efficient inverter operation with a relatively simple power circuit. The rectified output voltage wave as it appears at the input terminals of the output filter is illustrated in Figure 5. Two immediately apparent properties

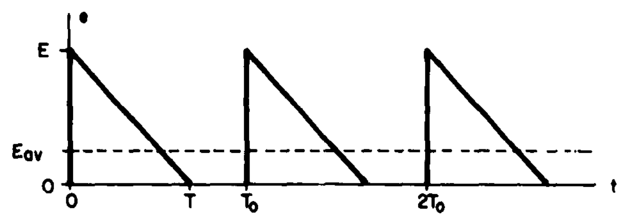

Figure 5. Rectified output voltage wave of FM-SS modulator

of this voltage wave require consideration at this time. First, the relatively high harmonic content, when considering the output filter size, makes it necessary to justify the use of such a wave by the high speed of filter operation, e.g., the order of 5 kc. The filter size decreases essentially with the square of the operating frequency, and when this is compared to the conventional 800 or 120 cps, then an attenuation ratio of about 150 or 1600 is gained that will comfortably allow the increase of harmonic content by a factor of, say, approximately three, leaving an adjusted reduction of output filter size of about 50 or 500 respectively. In cases of operation from an ac supply line, the question of filtering of the hf ripple will in general become negligible compared with the requirements of the time varying input signal and possibly the lf ripple caused by the supply source. The second apparent property is the lack of control over the waveform of the on-period. Once the cycle has started for a given inverter, driven from a given source E and feeding a given load R_L, this cycle will complete itself with no provisions for control This lack of control over the individual on-period is the price paid for high efficiency operation of the turn-off mechanism.

This latter property of the output voltage wave suggests a means of control of the average output voltage by variation of the time interval between succeeding on-periods, as described with reference to Figure 2b on page 4 being the characteristic operation of the frequency modulated self-stabilizing amplifier. Assume that one condition, the magnitude of E, deviates from a nominal value E_1, then the triangles as shown in

Figure 5 will change their volt seconds area I from

$$I_1 = \frac{E_1 T_1}{2} \tag{3a}$$

to

$$I = \frac{E T}{2} \tag{3b}$$

where T_1 is the nominal on-period corresponding to a source voltage E_1. The slope of the triangle remains unchanged for a given load, provided the average output voltage is maintained, since the load current is unaltered, as expressed by relation (1). When, e.g., $E > E_1$ then $T > T_1$ for constant c de/dt, and

$$I/I_1 = E^2/E_1^{\,2} \tag{4}$$

since T and T_1 respectively are linear functions of E and E_1 respectively.

It is desired that

$$\frac{I}{T_o} = K = E_{av} \tag{5}$$

for constant output voltage, i.e., T_o will have to vary linearly proportional to I. If this is to be implemented by volt-time integration then there will have to exist some operating voltage source when $T \geq t \geq T_o$ in the read-out (set) circuit, unlike the case when the on-cycle is terminated by the control circuit. A control circuit analogous to a volt-second reset (6) circuit is considered with a proper modification for the just-mentioned necessary additional voltage source. Switches S_1 and S_2 are operating out of phase with equal period T_o each under conditions of cycle stability. During period T_{o1} switch S_1 is closed and switch S_2 open; saturable reactor SR is being reset by $E_R\, T_{o1}$ volt seconds. During period T_{o2} switch S_1 is open and switch S_2 is closed: saturable reactor SR undergoes a readout (set) procedure

$$E_o\, T_{o2} - \int_0^T e\, dt$$

until it saturates and a signal e_t appears at terminals ab as shown in Figure 6. Voltage e is introduced into the set circuit with proper polarity by a control winding on the main transformer T. The wave shape that appears on the saturable reactor terminal, when referred to volts per turn is illustrated in Figure 7, while maintaining, for simplicity, the previously used voltage notations. By virtue of the basic property of saturable reactors

$$E_R \cdot T_o = E_o\, T_o - \int_0^T e\, dt = E_o\, T_o - I \qquad T_{o1} = T_{o2} = T_o \tag{6}$$

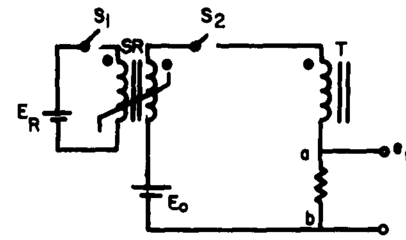

Figure 6. One-half of modified volt seconds reset for FM-SS modulator

or re-expressed

$$\frac{I}{T_0} = E_0 - E_R = E_{av} = K \tag{7}$$

as desired. This relation will hold independent of $e = f(E, R_L, C)$, as being independent of the shape of the output wave form, as long as it conforms to the proper limitations. It will hold also notwithstanding variations of magnetic properties of SR due to changes in temperature, as described in the literature concerning volt seconds reset.[4]

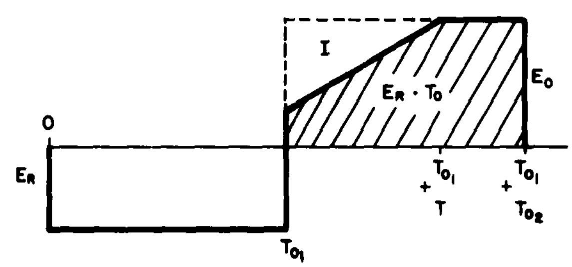

Figure 7. Voltage waveform on saturable reactor SR

The type of operation, just discussed, can be considered as a succession of periods T_O of operation in which each period is initiated at the termination of the preceding period, and the duration of that period T_O is a variable, linearly proportional to the magnitude of the volt time integral I of the output voltage time wave. This interaction between starting mechanism of individual periods T_O and the dependence of the duration of these periods T_O upon the output voltage wave form points to a relaxation oscillator type operation of the system, of which the power circuit is an essential part.

The operation of the control mechanism is illustrated by a block diagram as shown in Figure 8. The bistable multivibrator will activate switching operations as indicated symbolically with discussion of the control circuit as shown in Figure 6.

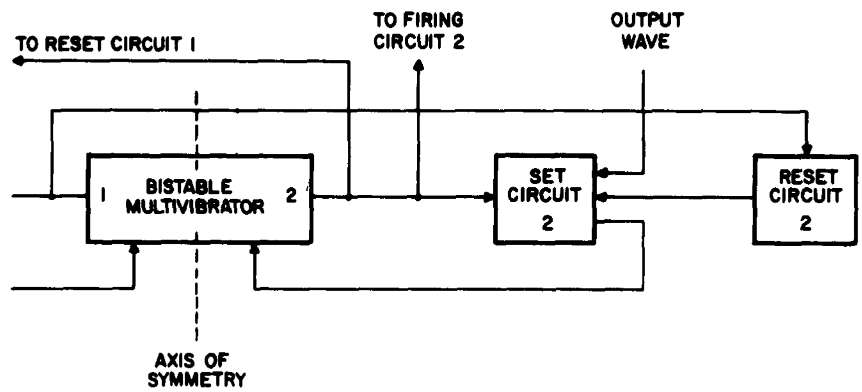

Figure 8. Symbolic block diagram of control circuit for FM-SS modulator

Output 1 activates switch S_1 and output 2 activates switch S_2, while each of these switches is located within the respective block. Let an output be present at terminal 2 of the multivibrator. Then set circuit 2 is reading out, while reset circuit 1 is resetting and CR_2 is on. After CR_2 turns off and the previously discussed integration is completed in set circuit 2, a signal will appear at its output terminals (ab in Figure 6) and trigger stage 2 of the multivibrator into conduction, thus turning its output off, while simultaneously turning output 1 on. Output 1 will now activate set circuit 1, reset circuit 2 and firing circuit 1. The latter will emit a trigger pulse to turn on CR_1 at the initiation of this cycle, and the power transformer will feed the output wave to set circuit 1. Under conditions of cyclic stability an operation of set and reset as depicted in Figure 7 will ensue, thus leading to an operation as described, i.e., the power circuit will produce an output voltage, as determined solely by sources E_o and E_R in conformity with relation (7) and within design limits.

C. Design Considerations

A brief survey will be given to considerations of design of the power circuit and its components (Figure 3 , with the following symbols:

P_i	the input power
E	the input voltage
$I_{i_{av}}$	the average input current
I_i	the instantaneous input current
C	the capacitor in Figure 3
e_c	the voltage on capacitor C
P_o	the output power

E_{av} the average output voltage

$I_{o_{av}}$ the average output current

T the duration of the on-period

T_o the duration of one entire half wave inverter period

Consider an ideal system, for the time being, i.e., $P_o = P_i$. This circuit derives current from the source when CR_1 is on, i.e., $0 \leq t \leq T$; it is not connected to the source when CR_2 is on, but the energy stored in capacitor C is discharged. Thus

$$P_i = \frac{T}{2\,T_o} \; E\,I_i = E\,I_{i_{av}} \tag{8}$$

Following that

$$I_i = \frac{T_o}{T} \; \frac{2\,P_i}{E} = C \, \frac{de_c}{dt} = C \, \frac{E}{T} \tag{9}$$

with I_i being a constant, as shown before.

From here

$$C = T_o \, \frac{2\,P_i}{E^2} \tag{10}$$

Calling

$$f_o = 1/T_o$$

the latter expression can be rewritten as:

$$\frac{CE^2 f_o}{2} = P_i \tag{11}$$

which states in the well-known form that the product of the energy stored in the capacitor C - or its discharge - and the number of such operations per second f_o equals the power handled by the circuit. For example, if an amplifier should handle 250 watts from a 100-volt source at 2.5 kc speed of operation, $f_o = 5.10^3$, then

$$C = \frac{10^{-3}}{5} \quad \frac{500}{10^4} = 10\mu f$$

The same amplifier, when operating from a 200-volt source will require a capacitor of one-fourth that size, i.e., 2.5μf. Once the capacitor size has been established and the voltages E_O and E_R, as discussed before, are set, the frequency of operation will become a function of input voltage E and P_i (loading).

The average output voltage E_{av} is given by the relation:

$$E_{av} = \frac{1}{T_o} \quad \frac{E\ T}{2} \tag{12}$$

while the average output current, as supplied by the primary circuit can be formulated as

$$I_{o_{av}} = a \frac{T}{2T_o} I_i \tag{13}$$

where a is the power transformer turns ratio. Finally

$$P_o = \frac{E_{av}^{\ 2}}{R_L} = E_{av} I_{o_{av}} \tag{14}$$

The rms current in the primary transformer winding $I_{I\ rms}$ is readily expressed as:

$$I_{I\ rms} = I_i \sqrt{\frac{T}{2T_o}} \tag{15a}$$

$$= I_{i_{av}} \sqrt{\frac{2T_o}{T}} \tag{15b}$$

while the rms current in the secondary transformer winding(s) can be approximated as being equal to the average dc output current, i.e.,

$$I_{II\ rms} = I_{o_{av}} \tag{16}$$

The voltage drop on the semiconductors will vary with current, but not to the extent of purely resistive elements due to the nonlinear characteristics of controlled rectifiers and diodes. Thus the power loss in these devices will approach the product of average voltage and current. The characteristic operation of the FM-SS amplifier exposes the controlled rectifiers to only approximately one-half of the maximum forward and reverse voltage potentials, as compared to a common in-

verter with center tapped transformer, which exposes the switching elements to more than twice the source voltage. Thus one pair of controlled rectifiers rated for approximately 5 amperes average current and 400 volts (e.g., GE's C-10-D) could handle comfortably a power of 1.5 kw, when used in that configuration, though units with higher current ratings may be used for a larger margin.

The capacitor C will carry the load current, as shown before. However, it will not carry a commutation current, and a moderate amount of care in the choice of that capacitor (e.g., extended foil type) renders its losses virtually negligible.

Transformer and inductor design requires the proper considerations, applicable to hf power systems. Questions associated with conditions of no load affect transformer design and will be discussed in the succeeding quarterly report.

D. Active Filtering of the FM-SS Inverter

The rectified output wave of the FM-SS inverter will contain essentially two distinct sources of ripple: (1) the characteristic triangular hf wave followed by the inverter operation, and (2) a lf ripple that appears at the input terminals of the inverter when driven through a rectifier-filter from an ac source. The high ripple frequency will, in general, be a multiple of the low ripple frequency with ratios in the order of say 100 down to unity according to the frequency of operation of both the supply source and the inverter, as well as the number of phases available as supply source, and particulars of inverter design.

The inverter acts as an active filter by its intrinsic mode of operation, and this filtering action can be amplified by proper design to a virtual elimination of an incoming low frequency ripple. This property permits a reduction of the overall filter size of an ac to dc operation. A case will be considered in which a coarse filter will reduce the ripple on the rectifier voltage wave of an ac supply source, and further reduction of the source frequency, $2f_s$, ripple is desired. Consider an arrangement as indicated in Figure 1, repeated here for convenience. The inverter will accept the time-varying

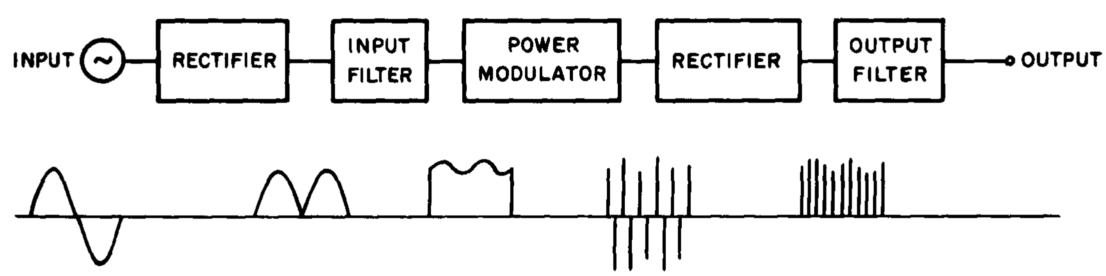

Figure 1. Successive voltage wave shaping

level of its input wave essentially as its dc voltage level during one cycle of operation if the ratio of the two frequencies involved $2f_s \cdot T_o$ is small enough , e.g., $2f_s \cdot T_o < 0.1$. This assumption will be used in the analysis to follow. The waveshape e_i at the input terminals of the inverter is resketched in Figure 9. The average value of e_i is E_i and the ripple amplitude is symbolized by A, such that

$$e_i = E_i + \epsilon(t) \tag{17}$$

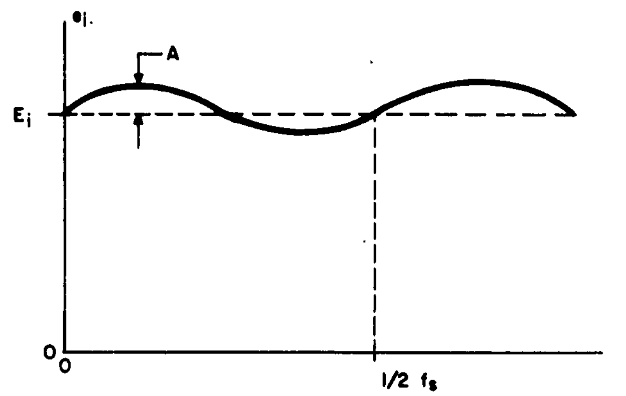

Figure 9. Inverter input voltage

The instantaneous value of the ripple voltage $\epsilon(t)$ is expressed as

$$\epsilon(t) = A \sin 4\pi f_s t \tag{18}$$

and the "constant" ripple voltage level during the n^{th} cycle of the inverter ϵ_n is given by:

$$\epsilon_n = A \sin 4\pi f_s \sum_{k=1}^{n-1} T_{ok} \tag{19}$$

where $k = 1, 2, \ldots, n - 1$; counting is started at a periodical point of e_i, e.g., where the ripple is zero and rising. T_{ok} is the symbol for each of the individual entire successive periods of operation of the inverter, where each period corresponds to the duration of one pulse emitted by the rectifier including its off time. This is illustrated in Figure 10, which shows the rectified output waveform of the inverter with superimposed input ripple.

The rms value of a voltage time curve gives a measure of the energy derived from it per unit of time by a passive, time-invarying network. Such a network is the output filter as indicated in Figure 1 followed by the load R_L. The rms value of the input voltage as shown in Figure 9 for one lf cycle $1/2f_s$ is defined as

$$e_{i\,rms} = \sqrt{2f_s \int_0^{1/2f_s} e_i^{\,2}\, dt} \tag{20a}$$

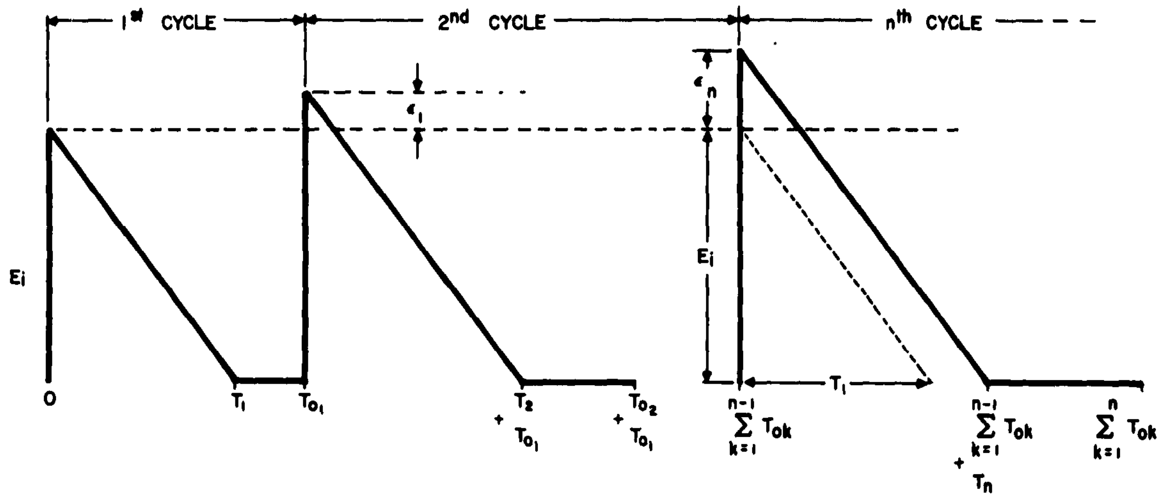

Figure 10. Rectified output waveform of the inverter with superimposed input ripple

or

$$e_{i\,rms} = \sqrt{2f_s \int_0^{1/2f_s} [E_i + A \sin 4\pi f_s t]^2 \, dt} \tag{20b}$$

and

$$e_{i\,rms} = \sqrt{[E_i^2 + A^2]/2} \tag{20c}$$

as expected. If it is desired to send a constant amount of energy into the input terminals of the output filter so that no variations in output voltage should occur, then this cannot be accomplished unless

$$\frac{de_i}{dt} = 0 \tag{21}$$

at any time, i.e., average voltage and rms voltage are identically equal at any time. While this applies to a pure dc free of ripple, it cannot be attained with the characteristic inverter operation involving an intermittent succession of triangular waveshapes. If, however, a condition of equal rms voltage derived from a unipolar voltage wave is fulfilled over each of the inverter cycles, then the successive inverter cycles will conform to the requirement of a ripple-free dc, when the time varying changes in these conditions within each cycle are ignored. The latter changes occur, however, with a periodicity corresponding to the inverter output frequency $1/T_O$, while variations in rms voltage at a lower frequency have been eliminated, so that, specifically, the $2f_s$ ripple is suppressed, and the filter-load network receives a constant flow of joules per unit of time when considering each cycle as a closed entity.

For the purpose of analysis it will be irrelevant which way the triangles face in the volt-time variations, and these triangles are rearranged for mathematical convenience as shown in Figure 11 without variance of their harmonic content. The n^{th} cycle is

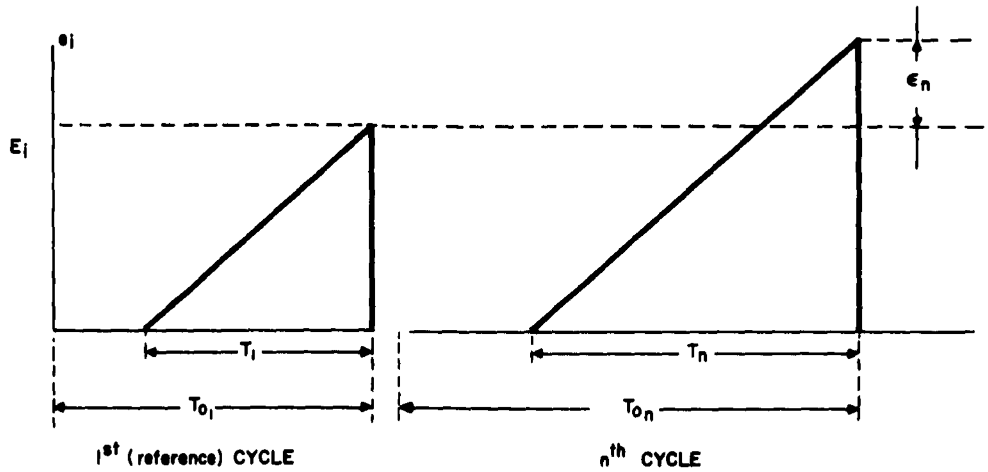

Figure 11. Rearranged inverter output voltage

any of the inverter cycles and the input voltage -- assumed constant over the entire cycle at this time -- is given by

$$e_i\left(\sum_{n=1}^{n} T_{ok}\right) \triangleq E_i + \epsilon_n \tag{22}$$

$$\epsilon_n = A \sin 4\pi f_s \sum_{n=1}^{n} T_{ok} \tag{19'}$$

with readjustment of sums of periods according to the direction of triangle orientation. (The symbol $e_i\left(\sum_{k=1}^{n} T_{ok}\right)$ means $e_i(t)$ at $t = \sum_{k=1}^{n} T_{ok}$.)

The rms voltage of the first (reference) cycle is given by

$$e_{1.rms} = \sqrt{\frac{1}{T_{o1}} \int_0^{T_{o1}} E^2 \frac{t^2}{T_1^2}\, dt} = E_1 \sqrt{\frac{T_1}{3T_{o1}}} \tag{23}$$

and the rms voltage for any arbitrary n^{th} cycle is given by

$$e_{n\,rms} = (E_i + \epsilon_n) \sqrt{T_n/3T_{on}} \tag{24}$$

If the energy per unit of time carried by the first and the n^{th} cycle over the entire respective period should be equal, then

$$(e_{i\,rms})^2 = (e_{n\,rms})^2 \tag{25a}$$

or

$$E_i^{\,2} \frac{T_i}{3T_{o1}} = (E_i + \epsilon_n)^2 \frac{T_n}{T_{on}} \tag{25b}$$

and

$$T_{on} = (1 + \frac{\epsilon_n}{E_i})^2 \, T_n \frac{T_{o1}}{T_1} \tag{26}$$

Since I_L' is a constant, it follows that

$$\frac{E_i + \epsilon_n}{T_n} = \frac{E_i}{T_1} \tag{27}$$

or

$$\frac{T_n}{T_1} = 1 + \frac{\epsilon_n}{E_i} \tag{28}$$

such that combining (26) and (28)

$$T_{on} = (1 + \frac{\epsilon_n}{E_i})^3 \, T_{o1} \tag{29}$$

T_{o1} is given by general design considerations -- largest load, smallest input voltage, and ripple variations -- and thus is known; so is E_i as the nominal input voltage and $\epsilon_{n\ max} = A$ as defined by equation (20b) and illustrated in Figure 9, as the amplitude of the lf ripple. Then

$$T_{on\,max} = (1 + \frac{A}{E_i})^3 \, T_{o1} \tag{30a}$$

This relation (30) states that if the control circuit is arranged in such a way that the said relation holds, there will be no low frequency ripple emitted by the FM-SS inverter into output filter and load, i.e., the amplifier -- operating as an active filter -- will have suppressed the low frequency ripple as supplied by the input filter completely. For completeness it is noted that

$$T_{on\,min} = (1 - \frac{A}{E_i})^3 \, T_{o1} \tag{30b}$$

For $|A/E_i| << 1$ can be written

$$T_{on\,max/min} \cong (1 \pm 3A/E_i)\, T_{o1} \tag{31}$$

with sufficient accuracy for engineering purposes.

The control circuit as illustrated in Figure 12 and its analysis shows that

$$E_o - E_R = \frac{T_n}{T_{on}} \frac{E_i + \epsilon_n}{2} = \frac{T_1}{T_{o1}} \frac{E_i}{2} \tag{32}$$

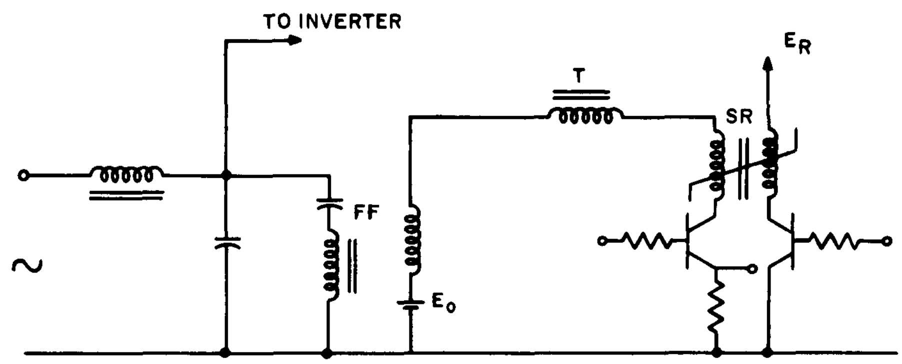

Figure 12. Ripple elimination signal generation and coupling

when applying the preceding terminology to expression (7) on page 13. Using relation (28) this is rewritten as:

$$T_{onr} = (1 + \epsilon_n/E_i)^2\, T_{o1} \tag{33}$$

where T_{onr} stands for "ripple"-T_{on}. The ratio

$$r_n \triangleq \frac{T_{on}}{T_{onr}} \cong (1 + \epsilon_n/E_i) \tag{34}$$

when considering relations (29) and (33). This latter relation (34) expresses the fact that T_{on} for lf ripple-free operation in the output filter is attained when the nonadjusted period T_{on} as given by relation (33) is modified by a ratio r_n as given by relation (34). This is implemented by derivation of a ripple signal from the input filter capacitor via a feed forward transformer FF which will add a desired fraction of the input voltage ripple to the readout voltage E_o and thus provide the additional adjustment of T_{onr} as required by relation (34) to its desired duration T_{on}. While a complete elimination of

the low frequency ripple may not be attainable due to the shortcomings of physical implementations and side effects, it is expected -- and has so far been confirmed experimentally -- that the FM-SS inverter provides appreciable lf ripple attenuation by operating as an active filter.

E. Protective Features

The FM-SS inverter is readily protected against failure due to overload, output short circuit, or accidental malfunction of one of its power components. One potential source of failure is the malfunction of one of the power switches (controlled rectifiers), due to unusual transient conditions, etc. If, for any reason, one controlled rectifier fails to open, it will entail no more than that capacitor C as illustrated in Figure 1 is either completely charged or discharged while no dc path from source to ground exists through any of the controlled rectifiers, CR_1 or CR_2 respectively. This property distinguishes the RC-inverter and the FM-SS inverter from any other inverter using controlled rectifiers as power switches. In other words a failure of any one of the controlled rectifiers to open will in itself not cause a short circuit, followed by a derangement or a destruction of components. However, if one controlled rectifier were not to open and continued to carry some current in excess of its holdir ; current, then a firing signal must be prevented from reaching the other controlleu rectifier gate, because a condition of simultaneous conduction of both controlled rectifiers would provide a short circuit path from source E to ground. This prevention of improper firing of controlled rectifiers is implemented by gating of the respective firing signals according to whether the controlled rectifier which is not to be fired has opened or not. In other words: the firing signals are gated in such a way that as long as one controlled rectifier is conducting, the other one cannot be fired even when the control circuit may emit a firing pulse. Gating circuits associated with each of the individual controlled rectifiers respectively will not clear the line of transmission for that pulse as long as the other controlled rectifier has not opened. This is illustrated in Figure 13 which shows the

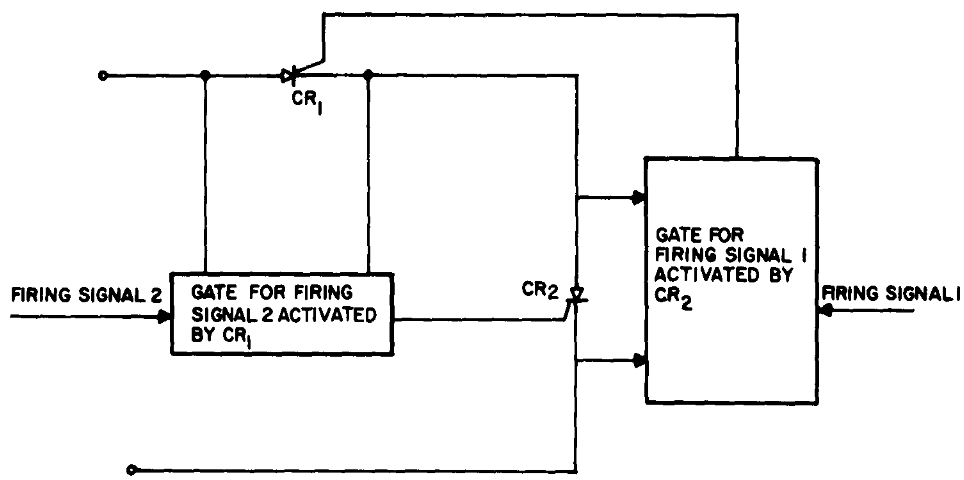

Figure 13. Symbolic diagram of protection mechanism

respective gates in block diagram form. These gates will transmit firing signals whenever the CR in control will be back-biased or exceed a minimum forward drop, thus excluding by a margin its state of conduction. This arrangement permits self-starting of the circuit when turned on, or when trying to resume operation after a temporary disturbance.

Another potential source of failure, that of overload including short circuited output, is met by suppression of the successive firing pulses for the duration of these conditions. A circuit including components C_d and R_d as shown in Figure 14 differentiates the voltage wave $e_c(t)$ on capacitor C as given by relation (2).

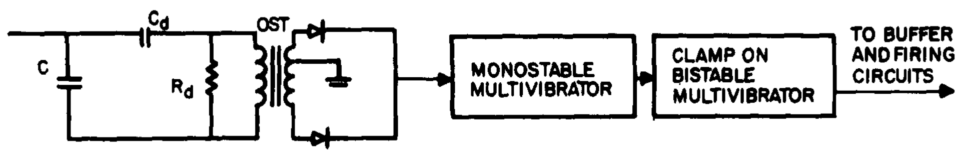

Figure 14. Overcurrent sensor and recycling clamp for driver circuit

This differentiated voltage $de_c/dt = I_L'/C$ is transmitted by overload signal transformer OST and a full wave rectifier into the input terminal of a monostable multivibrator. Whenever I_L'/C exceeds a certain predetermined threshold value then its equivalent rectified de_c/dt will rise to a level that triggers the monostable multivibrator into its quasi-stable state for a time T_{clamp}, e.g., five milliseconds. This circuit in turn will now energize a clamp that virtually grounds both output terminals of the bistable multivibrator that dominates the inverter control circuit as illustrated in Figure 8. In this condition the entire relaxation power oscillator will cease operation until the monostable multivibrator under discussion after elapse of the time T_{clamp} returns to its stable state and de-energizes the clamp. The bistable multivibrator resumes operation and energizes the proper firing circuit, getting one inverter cycle started. If an overload or a short circuited output persists then de_c/dt will again exceed the predetermined threshold value and after a recovery time $T_{recovery}$ of the monostable multivibrator another cycle of clamping and then releasing of the control circuit will ensue, etc. This will continue until the cause of faulty operation is removed. Once the peak value of de_c/dt remains below that threshold, the system will resume normal operation. The ratio $T_{clamp}/T_{recovery}$ should be in the order of, say, several hundred to: (a) restrict the number of power pulses per second into the overloaded or short circuited system below a safe limit and (b) reapply the clamp (if necessary) within the duration of the first short circuit current pulse, i.e., within microseconds.

Another less severe problem arises with insufficient loading. This can be solved by applicable dynamic modification of R_L and/or C including proper transformer design.

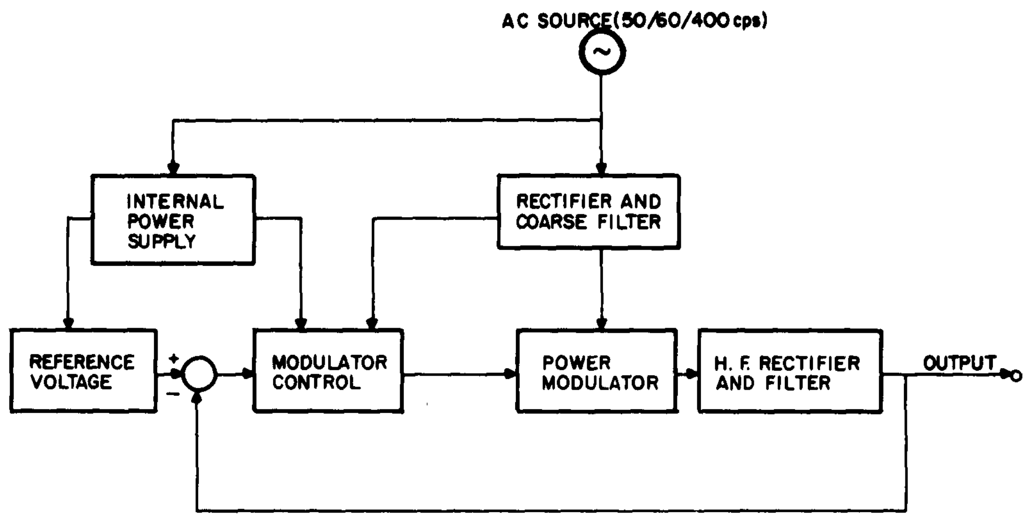

Figure 15. Block diagram of the complete system

F. Tap Switch Modulation Technique

A detailed study of reduction of harmonic content by tap switch modulation was carried out along the principles as stated in the proposal to this program. A modification of the circuit shown in that proposal was studied.

In this circuit high frequency conversion is obtained by applying the input voltage to alternate ends of the same primary winding at the conversion frequency. Tap switching is accomplished by sequential switching of the connections between the four sections of the primary winding as shown in Figure 16. As may be seen by inspection of this figure the effective turns ratio of the parallel-series and series configurations are one-half and one-fourth respectively of the parallel configuration. Thus, if the configuration is changed from parallel to parallel-series, and then to series as the instantaneous input voltage goes from zero to its peak and in a reverse fashion as the voltage returns to zero, a chopped envelope of the high frequency output results. Regulation is obtained by variation of the times at which the configuration switching takes place.

The ensuing rectifier output wave form is shown in Figure 17. The Fourier coefficients of this dc wave form with quarter symmetry appear only as those of the even harmonics of the cosine series. The angles of switching θ_1 and θ_2, involving the step-varying transformer ratios add more independent variables to the evaluation of these coefficients for the purpose of reduction of the harmonic content. These coefficients were investigated in that sense, yielding an insight that by use of a minimum of power transistors that would withstand at times 80 volts each, 30 or 41 units will be needed to reduce the overall filter size and weight to one-third of the conventional values as compared to ordinary 50-cps power supply design.

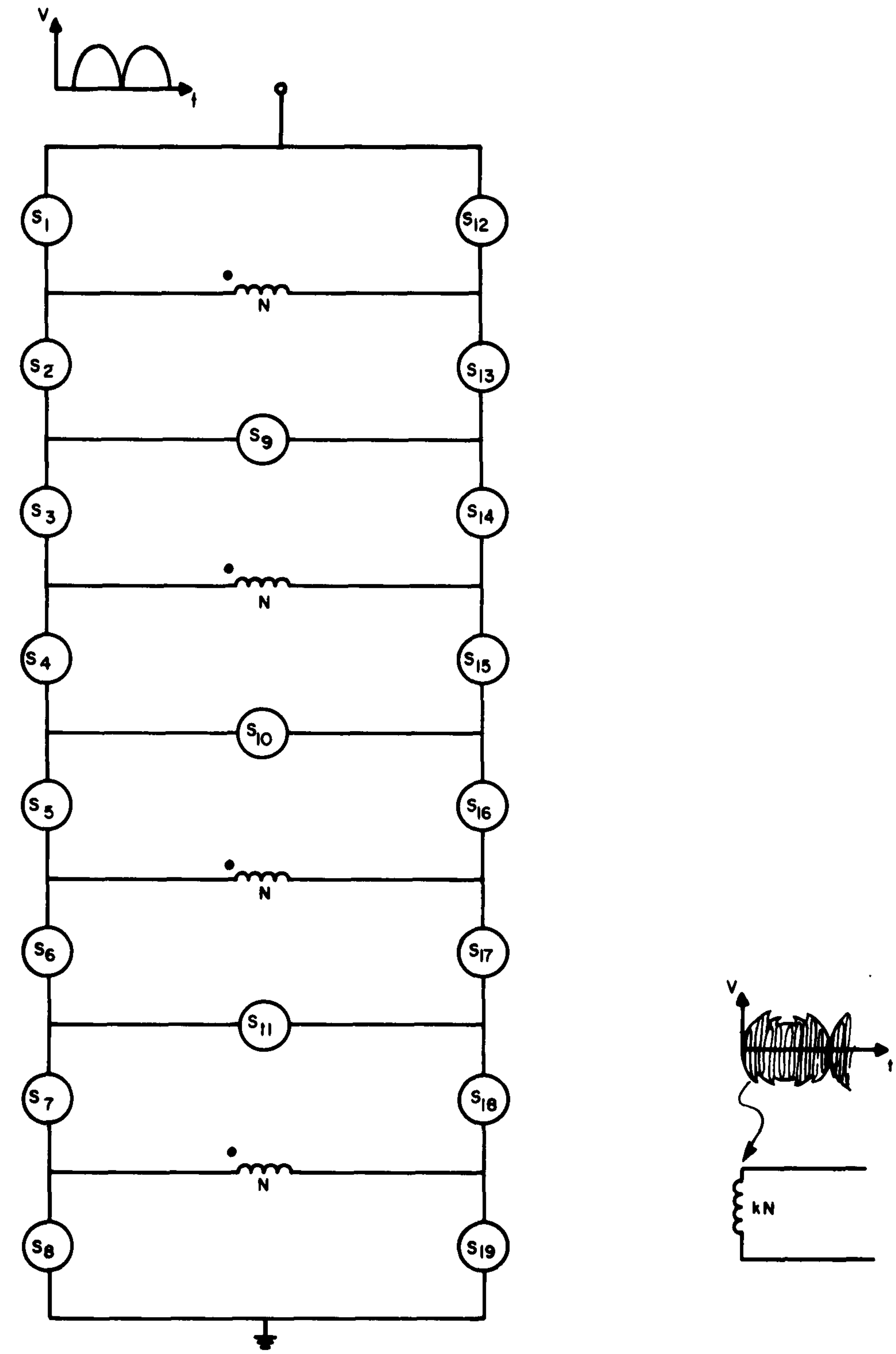

Figure 16. Tap switch modulation circuit

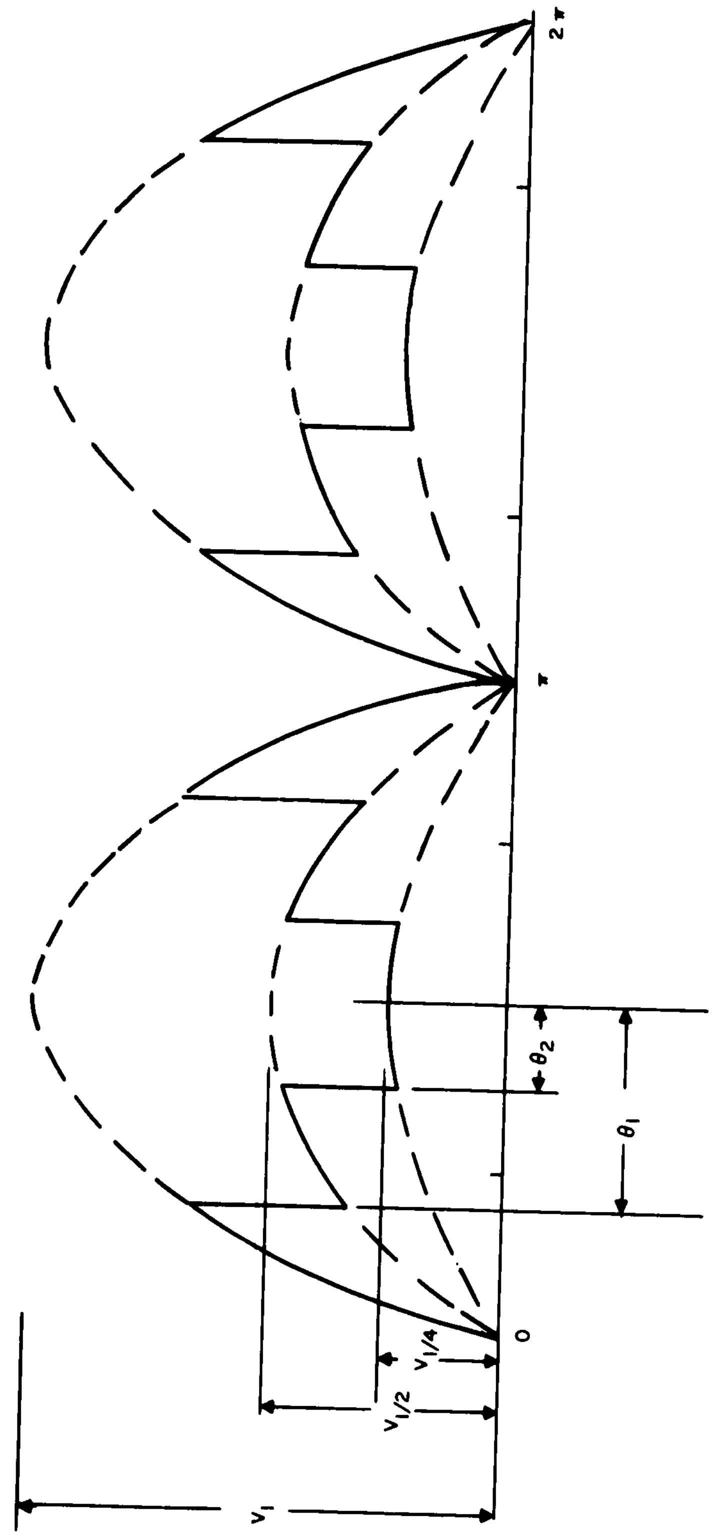

Figure 17. Rectified tap switch modulated output wave

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V. CONCLUSIONS

The first study phase on this project showed that it is possible to reduce substantially weight and size of dc power supplies operating from a 50-cps ac source by use of inversion techniques without impairment of quality of performance. The FM-SS inverter, as described in this report, shows a relatively simple power circuit, and offers the added advantages of being self-stabilizing, self-protecting, and operating as an active filter section with respect to the ripple caused by the supply source. Other features, such as automatic controlled rectifier turn-off, the absence of commutation currents and useful storage of essentially all not immediately used energies present in the system, indicate a favorable efficiency of operation. The breadboard, comprising inverter, output rectifier, and filter, has been operating at a power level in excess of 200 watts and shows efficiencies in excess of 80 percent with about 90 percent efficiency of inverter operation. An estimate of the eventual efficiency of operation should become available when an evaluation of a further completed breadboard is made. Provisions exist so that overload and short circuit should not damage the power supply, while preparations are under way to test designs for safe unloading of this supply. Specifications concerning regulation and ripple are expected to be met.

VI. PROGRAM FOR NEXT INTERVAL

Work will be continued toward specific designs as called for by the program. Existing circuits will be further studied, tested, and improved toward use in the experimental models. Features, such as lf ripple suppressions, overload protection, unloading provisions, input filter, etc., will be developed and incorporated into the breadboard. Design of power components will be initiated. A breadboard will be built to conform to the essential requirements of the program (Item 2), and susceptible to modifications (Items 3).

VII. IDENTIFICATION OF PERSONNEL

A. Key Personnel in Ithaca

E. W. Manteuffel

Dr. Manteuffel was awarded the Diploma-Ing. in 1929 and the Dr.-Ing. (DSC) degree in 1941 by the University of Darmstadt, Germany.

He was an instructor in the Institute for Electric Machines, University of Darmstadt, in 1930 and 1931, an Assistant Professor in the Institute for Electric Power Transmission and Power Plants from 1931 to 1934, and Assistant Professor in the in the Institute for Electric Power Plants and Electrical Apparatus from 1934 to 1936, where he solved several theoretical and experimental problems on ac commutator generators and pseudoharmonic oscillations, and designed special electric devices (e.g., continuously regulated transformer).

Dr. Manteuffel was a Development Engineer at Brown Boveri and Cie, A. G. Mannheim, Germany, where he developed and tested electrical apparatus and automatic control systems for electric locomotives and multiple unit motor-car trains from 1936 to 1940. During the period from 1940 to 1945, he was chief of the Development Laboratory for electrical apparatus and control systems for electric locomotives and chief of the Design Section for electrical apparatus for locomotives, streetcars, and trolley buses. During this time he developed a novel system for regenerative ac braking of electric locomotives, different solid state regulators employing magnetic amplifiers, e.g., voltage, power factor and current regulators. In 1946 and 1947 he was Consulting Engineer, being engaged in further development of magnetic amplifiers and the development of a solid state regulator for lighting machines in railroad cars. During his employment with Brown Boveri he was granted nine patents.

From 1947 to 1950 he was a Special Employee of the Ordnance Research and Development Division, Suboffice (Rocket), Department of the Army, Fort Bliss, Texas. He designed special apparatus and developed single and multistage magnetic amplifiers for missile applications.

Dr. Manteuffel was Deputy Chief, from 1950 to 1953, of the Research Laboratory, Guidance and Control Branch, Ordnance Guided Missile Center, Redstone Arsenal, Huntsville, Alabama, where he developed magnetic amplifiers, magnetic frequency doublers, magnetic voltage stabilizers, a magnetic mixing computer, and a frequency and voltage regulator of extremely high accuracy.

Since 1953, Dr. Manteuffel has been at the General Electric Advanced Electronics Center at Cornell University, where he is Consulting Engineer-Electrical Engineering in the Advanced Engineering Physics Subsection. He has technical leadership in investigations of magnetic circuits, including amplifiers, power supplies, modulators, and control systems. He has been granted two U. S. patents.

F. C. Schwarz

Mr. Schwarz attended technical universities in Germany and the Netherlands. In 1956, he received his MSEE from Columbia University. From 1956 to 1959 he did postgraduate work in Nonlinear Networks at Columbia University.

Since 1959, he has been working toward his doctorate in Electrical Engineering and Applied Mathematics at Cornell University.

Mr. Schwarz worked as independent consultant for servomechanism and automation from 1957 to 1959. He developed techniques in the field of automation of metal manufacturing processes.

He has been Project Engineer at General Electric's Advanced Electronics Center for the light weight, fast switching type power supply for the B-70 Radar Modulator. The project was preceded by invention and reduction to practice of pertinent techniques. He is responsible for development work on the ferro-resonant circuit, involving development and reduction to practice of new techniques for temperature and frequency stabilization of magnetic amplifiers. He has undertaken basic research of iron core devices leading to a substantial reduction in weight and size. He is also responsible for evaluation work in cryogenic electric engineering.

Mr. Schwarz is currently Project Engineer on the Switch Modulation Power Supply, for which he invented and reduced to practice the RC-inverter and the FM-SS inverter.

B. Key Personnel in Syracuse

D. A. Paynter

Dr. Paynter received his BS in Engineering Physics from Montana State College in 1950. He was awarded an MS and a PhD in Applied Science from the University of Cincinnati in 1952 and 1954, respectively. His Master's Thesis was entitled "An Amplifier for a Relay Type Servo System," and his Doctoral Dissertation was entitled, "Temperature Coefficient of the Heat of Immersion."

From 1950 to 1954, he was a University Research Fellow in Applied Sciences on an electromagnetic system for the measurement of speed of marine vessels. He also was concerned with an Air Force contract for the study of ice adhesion to surfaces. This work included measurement of the heats of immersion in a micro-calorimeter and their relation to the physical properties of a water-solid system.

In 1954, Dr. Paynter joined Advanced Circuits of the General Electric Electronics Laboratory. Since then he has been involved in research and development of: power transistor switching circuitry; medium and HF oscillator mixer work; television sweep circuits; audio amplifiers; and transistor power converters and regulators. He received the General Electric Managerial Award in 1956 for his development of solid state dc to dc converters.

He is a member of Tau Beta Pi, Sigma Xi, and Phi Kappa Phi. He is the holder of five patents: A Transistor Deflection Circuit; A Single Power Transistor dc to dc Converter; A Driver Stage for Transistor Horizontal Deflection Systems; A Stable Transistor Oscillator; and Base-Controlled Transistor Converters. He is co-author of Transistor Circuit Engineering, John Wiley and Sons, 1957; and has written the following papers: "An Unsymmetrical Square Wave Power Oscillator," IRE Transactions of the PG on Circuit Theory, March, 1956; "Series Tuned Methods in Transistor Radio Circuitry," IRE Transactions of the PG on Circuit Theory, September 1957; "Single Power Transistor Converter," Transistor Circuits Conference - University of Pennsylvania, February, 1956; "Transistor DC-DC Converters," Airborne Electronics Conference, Dayton, May, 1955; "A Transistor Power-Converter Amplifier," Solid State Circuits Conference, Philadelphia, February 1960.

F. King

Mr. King received the BS in Electrical Engineering from Tufts University in 1955.

After serving three years in the Navy as an engineering officer, he joined General Electric on the Engineering Program. His assignments included work on Polaris, a flight control system simulator, a magnetic shielding device, solving engineering problems on an analog computer and designing accessory test equipment, study of weapons effects and of ionized gas, transistor circuitry, and power transistor circuitry. He has completed the A and B courses and is presently in the Electronic C course.

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indicate a lightweight, reliable power supply with relatively high efficiency. Attenuation of the source ripple by a factor four was attained experimentally by active filtering of the FM-SS inverter, and there are efforts underway for further improvement. A reduction of size and weight of at least two-thirds, compared to a conventional power supply with equal performance and efficiency, is expected as a result of this program.

Problems arising from fast rising wave forms and high repetition rate in the output rectifier were overcome by proper choice of fast switching diodes and adequate circuitry. Other problems entailed by relatively light loading, in the order of 10 percent are being worked on presently.

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